Final Project Clocking Scheme

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CPU is Driven by a Clock

- Every CPU performs actions that are advanced by a clock
- The clock runs at some frequency and alternates between 0 and 1
- We are generating a clock that each CPU should use as its only clock
- The frequency of our clock can be altered by supplying a divider

The Memory Subsystem Generates Our Clocks

- Use **sysclk1** as the clock for your processor

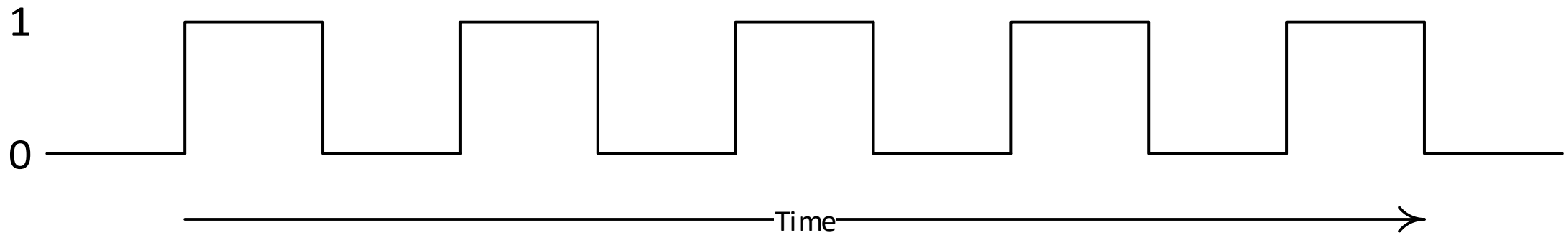
- Unfortunately, the clock divider for the memory subsystem extends the number of cycles the clock is kept low, but doesn't extend the time the clock is kept high
  - That is, the clock is not always a square wave

How **clock_divide_limit** Affects the Clock

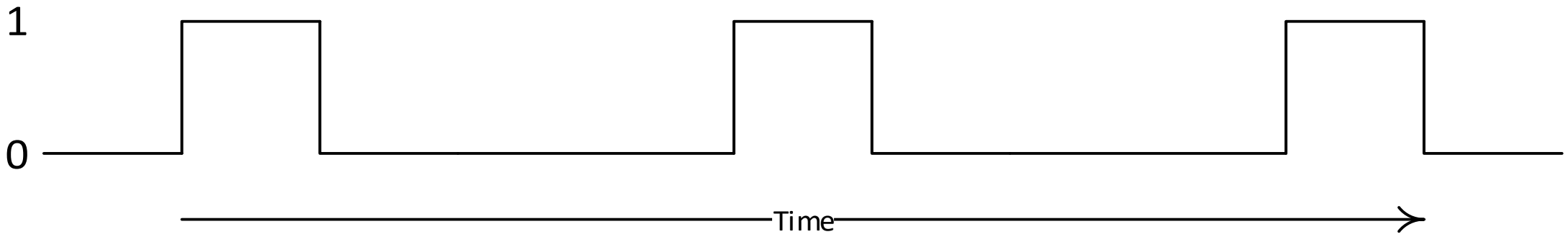
- If this value is non-zero, the generated clocks will be gated to zero for this number of cycles in between clock pulses
- If this value is zero (or left unmapped), the clocks are not gated

- Reminder: **DO NOT SET** THE LEAST SIGNIFICANT BIT of the **clock_divide_limit**

Full-Speed Clock



sysclk1 Clock with non-zero **clock_divide_limit**



Clock Components

- Each clock cycle has four distinct (and useful) components
  - The time the clock is 1
  - The falling edge of the clock
  - The time the clock is 0 (variable in duration)
  - The rising edge of the clock

- We will be using these components to enable actions in our CPU

Utilizing the Variable Time the Clock is Low

- The variable duration the clock is low will be used to adjust for the unknown propagation delay through combinational logic in your processor

- Therefore,
  - Use the falling edge of sysclk1 to transition the FSM to the next state
  - Use the rising edge of sysclk1 to clock registers

The Falling Edge

- When we detect a falling edge of the clock, we will advance the CPU's sequencer to its next state

The Time the Clock is Low

- During the time the clock is low, we will allow signals to propagate through combinational logic

- The time the clock is low must be long enough for the longest signal propagation path
- Fortunately, we are able to adjust the duration of time the clock is low

The Rising Edge

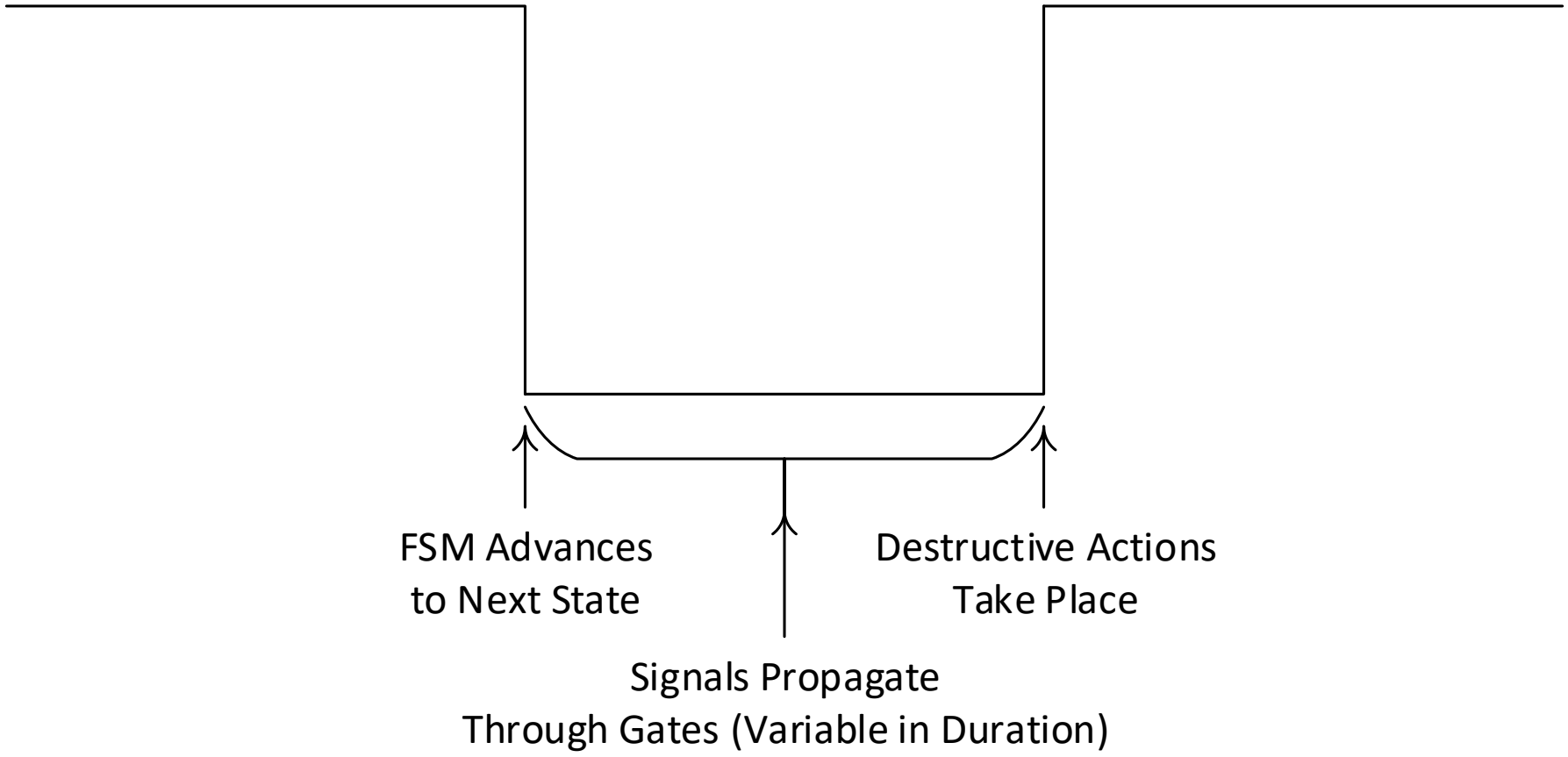
- When we detect a rising edge of the clock, we will perform all destructive actions
  - We will cause enabled registers to be loaded with new values

- The clock is run directly to the clock input of every register
- When appropriate for a particular action or instruction, the enable line for each register is set high when the clock is low
- If the enable line is set, the register is loaded on the rising edge of the clock

The Time the Clock is High

- The FSM determines its next state
  - The next state must be ready to be loaded into the FSM state register on the subsequent falling edge

Clock Detail



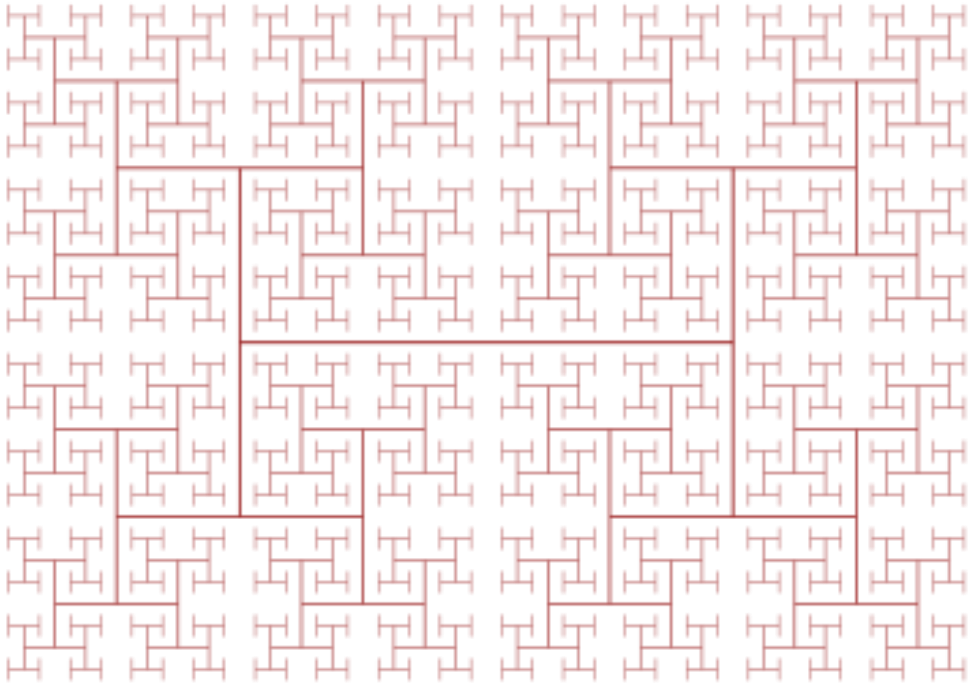
One Small Hiccup

- When the processor initially starts execution after being reset, the first clock edge is a rising edge
  - We do not want any destructive events to happen on this *first* rising edge

- So, the first state in the sequencer FSM should be an **idle** state that does not assert any enable control lines

Clock Distribution on FPGAs

- Uses an H-tree distribution network to ensure that the clock arrives at all flip-flops at approximately the same time



Clock Arrival Time Discrepancies

- Clock skew: arrival time differences because of trace length to different flip-flops
- Clock jitter: arrival time differences to each flip-flop because of instability of generated clock frequency (oscillator, phase-locked loop, temperature factors, crosstalk)

DE2-70 (EP2C70) Column Pins Clock Timing

Table 5–33. EP2C70 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.914	3.105	3.174	ns
t_{COUT}	1.589	1.666	2.948	3.137	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.27	0.268	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.304	0.3	0.118	ns

DE2-70 (EP2C70) Column Pins Clock Timing

Table 5–34. EP2C70 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.753	2.927	3.010	ns
t_{COUT}	1.465	1.535	2.769	2.940	3.018	ns
t_{PLLCIN}	–0.261	–0.276	0.109	0.09	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	0.125	0.103	–0.067	ns

DE2-70 (EP2C70) Inter-clock Network Clock Skew

Clock Network Skew Adders

Table 5–35 shows the clock network specifications.

Table 5–35. Clock Network Specifications

Name	Description	Max	Unit
Clock skew adder EP2C5/A, EP2C8/A *(1)*	Inter-clock network, same bank	±88	ps
	Inter-clock network, same side and entire chip	±88	ps
Clock skew adder EP2C15A, EP2C20/A, EP2C35, EP2C50, EP2C70 *(1)*	Inter-clock network, same bank	±118	ps
	Inter-clock network, same side and entire chip	±138	ps

Note to Table 5–35:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.